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# TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/646,289
Filing Date	August 21, 2003
First Named Inventor	Son Ho et al.
Art Unit	2188
Examiner Name	Kaushikkumar M. Patel
Attorney Docket Number	MP0390.I

Total Number of Pages in This Submission

## ENCLOSURES (check all that apply)

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Remarks  
The Commissioner is hereby authorized to charge any additional fees that may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 08-0750. A duplicate copy of this sheet is enclosed.

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Harness, Dickey & Pierce, P.L.C.		
Signature			
Printed name	Michael D. Wiggins		
Date	June 30, 2008	Reg. No.	34,754

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Signature		Date	June 30, 2008

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EM 184 988 147 US



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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Harness, Dickey & Pierce, P.L.C.		
Signature			
Printed name	Michael D. Wiggins		
Date	June 30, 2008	Reg. No.	34,754

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MP0390.I

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. \_\_\_\_\_

Application No.: 10/646,289  
Filing Date: August 21, 2003  
Appellants: Son Ho et al.  
Conf. No.: 9390  
Group Art Unit: 2188  
Examiner: Kaushikkumar Patel  
Title: LINE CACHE CONTROLLER WITH LOOKAHEAD

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**REPLY BRIEF TO THE EXAMINER'S ANSWER**

Mail Stop Appeal Brief-Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

June 30, 2008

Sir:

This reply brief is a reply to the Examiner's Answer mailed April 29, 2008, in the appeal from the decision of the Patent Examiner dated May 7, 2007, rejecting claims 1-2, 4-7, 9-10, 12-15, and 17-33.

### **STATUS OF THE CLAIMS**

A statement identifying the status of the claims is contained in the Appeal Brief.

### **GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

A statement identifying the grounds of rejection to be reviewed on appeal is contained in the Appeal Brief.

### **ARGUMENTS**

#### **Independent Claims 1, 5, 10, 13, and 18**

With respect to claim 1, Appellants respectfully submit that Zaidi, either alone or in combination with Jeddeloh and Loafman, fail to at least show, teach, or suggest a line cache including a plurality of pages that are accessed by the first CPU and a first memory device that stores data that is loaded into said line cache when a miss occurs, wherein when said miss occurs **and before a second miss occurs**, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one. Loafman appears to disclose that at least two misses occur before prefetching data from multiple sequential memory locations.

The Examiner acknowledges that none of the cited references explicitly teach this limitation, and states "the Examiner agrees with Appellants' argument that none of the references explicitly teach pre-fetching/loading n pages of the data on a single miss (i.e. before second miss occurs)." Instead, the Examiner alleges that "data pre-fetching or read-ahead is a very well known technique used in the art to reduce the number of page faults or cache misses, and continues to note that Loafman discloses that applications can read data either randomly or sequentially. The Examiner further acknowledges that "Loafman requires two page faults...to determine whether the

program is reading data sequentially.” In other words, Loafman discloses retrieving consecutive pages after observing a pattern of successive page accesses. As such, at least two misses are required. Accordingly, Appellants respectfully submit that the Examiner still fails to provide any reference that discloses loading sequential pages of a line cache with data from sequential locations in a first memory device when a miss occurs and before a second miss occurs.

While Appellants recognize that the Examiner is entitled to support a rejection based on common knowledge in the art, Applicant respectfully submits that the Examiner can only take official notice of facts outside of the record which are capable of instant and unquestionable demonstration of being “well-known” in the art. In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970). In the present case, none of the cited references disclose loading sequential pages of a line cache with data from sequential locations in a first memory device when a miss occurs and before a second miss occurs, as recited in claim 1. If the Examiner is basing the rejection on personal facts and/or knowledge, Appellants respectfully request that the Examiner provide an affidavit to support those facts. See MPEP 2144.03; 37 CFR 1.104(d)(2).

Appellants respectfully submit that the combination of Zaidi and Loafman appear to be absent of any teaching or suggestion of loading multiple pages of the line cache from sequential memory locations in response to a cache miss and before a second cache miss. Accordingly, Appellants respectfully submit that claim 1, as well as its dependent claims, should be in condition for allowance for at least the above reasons. Claims 10, 5, 13, and 18, as well as their corresponding dependent claims, should be in condition for allowance for at least similar reasons.

Similarly, with respect to claim 26, Appellants respectfully submit that Zaidi, either alone or in combination with Jeddeloh and Loafman, fail to at least show, teach, or suggest that **after a first time** that said requested data is not present in said cache, *n* pages of said cache are loaded with data from sequential locations of one of said first and second memory devices **to prevent any additional cache misses** for as long as sequential memory locations of said one of said first and second memory devices are addressed. Instead, Loafman appears to disclose that at least two misses occur before prefetching data from multiple sequential memory locations.

As described above with respect to claim 1, the Loafman still fails to disclose preventing any additional cache misses, and instead discloses retrieving consecutive pages after observing a pattern of successive page accesses (i.e. misses). Accordingly, Appellants respectfully submit that the Examiner still fails to provide any reference that discloses loading data from sequential locations of memory after a first miss to prevent any additional cache misses.

Appellants respectfully submit that the combination of Zaidi and Loafman appear to be absent of any teaching or suggestion of loading multiple pages of the line cache from sequential memory locations in response to a cache miss and before a second cache miss. Accordingly, Appellants respectfully submit that claim 26, as well as its dependent claims, should be in condition for allowance for at least the above reasons.

**CONCLUSION**

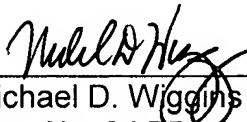
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Damian M. Aquino, Reg. No. 54,964, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNES, DICKEY, & PIERCE, P.L.C.

By:

  
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Michael D. Wiggins  
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MDW/DMA/dms

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